AN EXPERIMENTAL PULSE GENERATOR TO TEST THE EFFECT OF ALTERNATIVE PULSES DURING THE PRE-IGNITION PHASE, IN EDM

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ABSTRACT: The paper presents the structure of an experimental pulse generator destined to test the effect of an electric field, generated by alternative voltage pulses, on the ignition process in EDM. The goal of experiments is to validate the conclusions of a mathematic model describing this phenomenon. The principle of the power circuit and the block-diagram of the control unit are described. A state diagram is conceived, to implement the appropriate operation mode of this pulse source. An implement solution using a complex programmable logic device (CPLD) is presented.

KEYWORDS : EDM, PULSE GENERATOR, DIELECTRIC LIQUID, IGNITION

1. GENERAL STRUCTURE

The general design comes to test the effect of an electric field, generated by alternative voltage pulses in the ignition process of EDM [5],[1]. This new design comes to enlarge the investigation possibilities of an experimental pulse generator [2, 3] previously realized at the Non Conventional Technologies Research Center of the "Lucian Blaga" University of Sibiu.

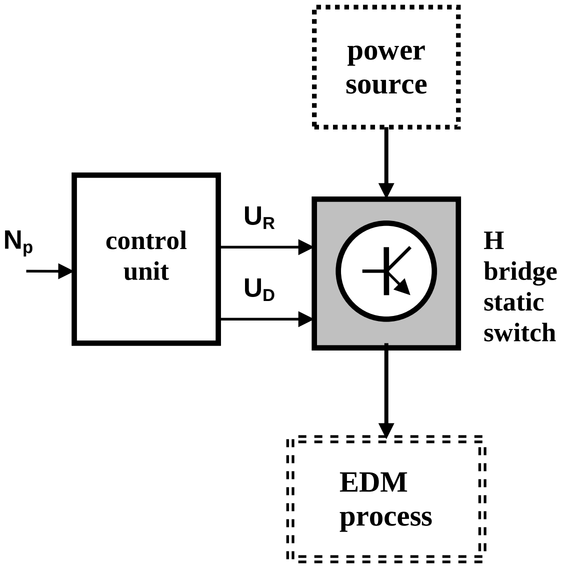

Fig.1 ***General structure of the pulse generator***

The pulse generator (Fig.1) uses an H bridge static power switch driven by a digital control unit, able to modify the number of pulses (**N_p**) in a programmed train.

2. POWER CIRCUIT UNIT

The general design of the power circuit (Fig. 2) is based on a H bridge, which is built with four static solid-state switches.

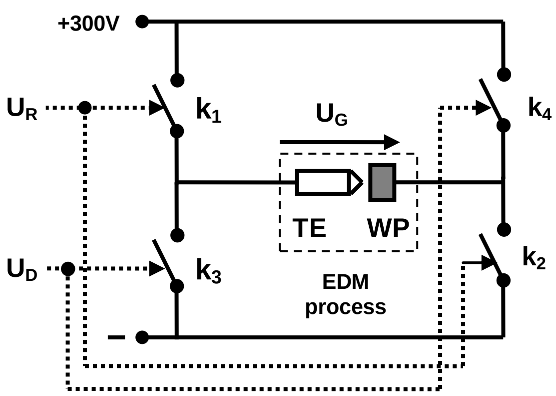

Fig.2 ***General design of power circuit***

The timing diagram of the input signals U_R ,U_D and command signal U_G is presented in Fig. 3.

If U_R is positive and U_D is zero, the switches k_1 and k_2 are closed (k_3 and k_4 are open), a positive voltage U_G will be applied across the EDM.

If U_R is zero and U_D is positive, the switches k_3 and k_4 are closed (k_1 and k_4 are open), a negative voltage U_G will be applied on the EDM process.

3. TIMING PARAMETERS OF THE COMMAND SIGNAL

The waveforms generated by the control unit are presented in Fig. 3.

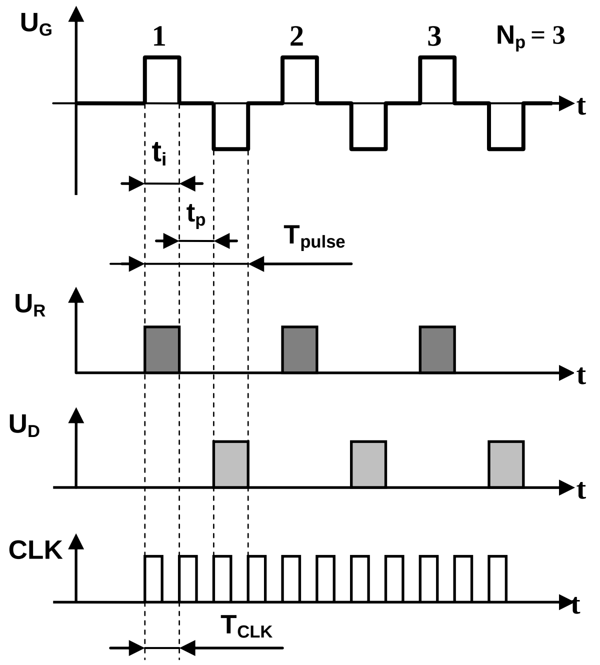

Fig.3 ***Timing parameters of the command signal***

The parameters of the signals are:

- t_i : pulse duration [s],
- t_p : pause duration [s],
- T_{pulse} : cycle duration (period) of the command signal U_G [s],
- T_{CLK} : cycle duration (period) of the pilot signal CLK [s],
- N_P : number of pulses in a train.

The period of the command signal is:

$$T_{PULSE} = 4 \cdot T_{CLK} \qquad (1)$$

The pulse and pause duration are :

$$t_i = t_p = \cdot T_{CLK} \qquad (2)$$

The value of the pause time t_P must be greater then the sum of the turn-on and turn-off delay time of the solid-state static switch.

3. THE CONTROL UNIT

The internal structure of the control unit is presented in Fig. 4.

The control unit delivers the input signals U_R, U_D (Fig. 3) to the power unit.

U_D and U_R are a train of programmable number of pulses (N_P). Input signal N_P is represented by a k bits number.

The operation of the control unit is dictated by a controller.

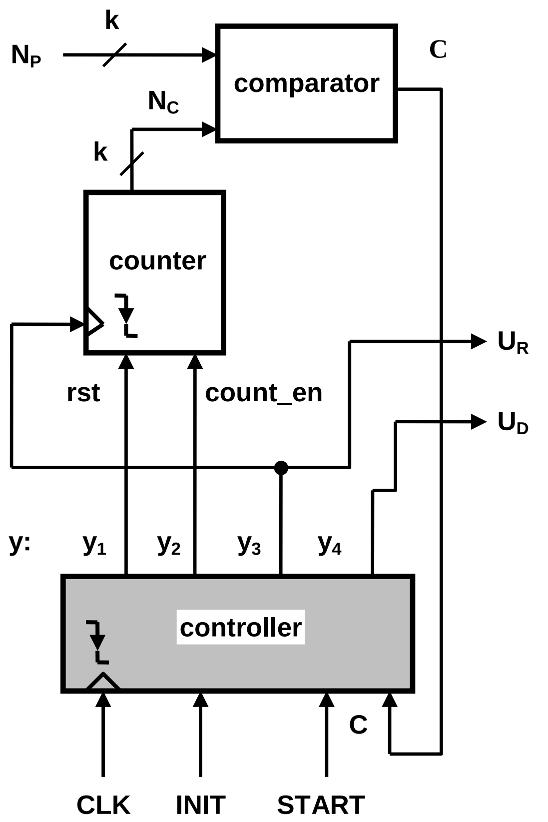

Fig.4 ***Block diagram of the control unit***

The input signals of the controller are:

- CLK : a pilot signal supplied by an external timing circuit,
- INIT: reset signal;
- START: enables the train of pulses.

The controller recycles (rst=1), enable the counter (count_en=1) and deliver the output signals U_R and U_D.

The timing parameters of U_R and U_D are in accord with equations (1) and (2).

The counter counts the number of U_R pulses. This comparator compares the N_P value to the number N_C. When $N_C \geq N_P$ the output signal of the comparator is C=0. This one acts on the controller who recycles the counter each time $N_C \geq N_P$. Fig. 5 presents the state diagram of the controller.

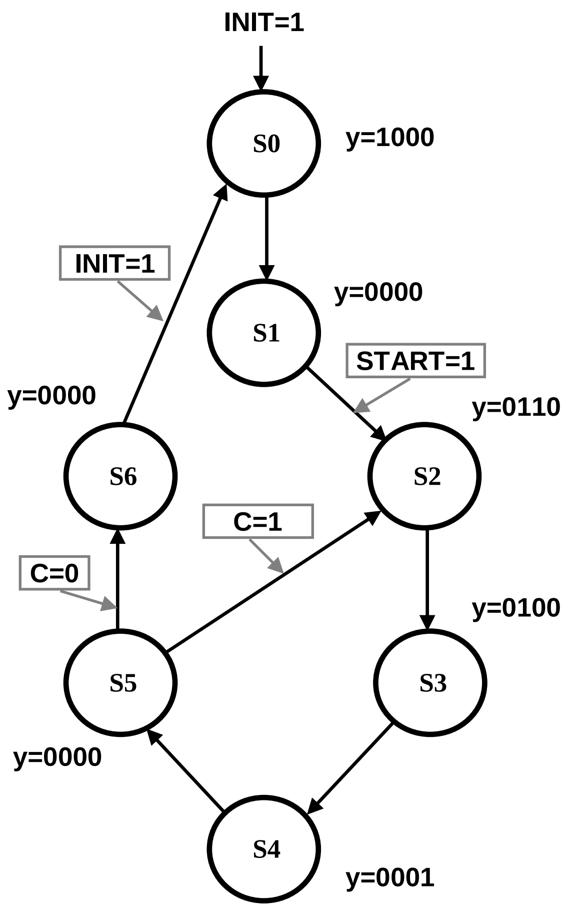

Fig. 5. ***State diagram of the controller***

The INIT external signal brings the controller in S0 state. In this state the counter is recycled by the **rst** bit. The controller passes in the stand by state S1.This state is maintained until START = 1. In S2 the counter is counting the number of U_R pulses (count_en=1). In the pause state S3, the counter is blocked. The U_D pulse is delivered in state S4.

In state S5, if the comparator delivers C=1 ($N_C < N_P$), the number of pulse N_C is less as the prescribed value N_P, the next state is S2. The generator continues to deliver pulses. Otherwise the controller goes to S6 and the pulse generator is stopped.

The controller is recycled when the INIT=1 command is applied.

4. BLOC DIAGRAM OF THE PULSE GENERATOR

The architecture of the pulse generator, containing the two previous presented blocks, is shown in Fig.7. START and INIT are general on/off signals and N_P releases the programmed pulse train.

5. SIMULATION AND IMPLEMENT

Fig.6 presents an example of simulation result: the control unit delivers a train of N_P=2 pulses.

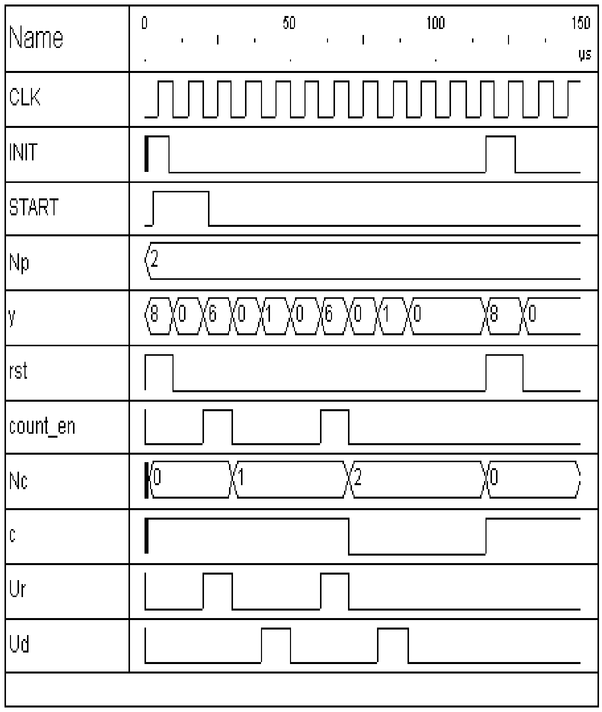

Fig. 6. ***Simulation result***

The design was realized using VHDL as hardware description language and WARP-6.3 as development tool [4]. The simulation tool was ALDEC-ActivHDLSim6.3. The target circuit was CY39100V676-200MBC, a high density CPLD made by Cypress Semiconductor.

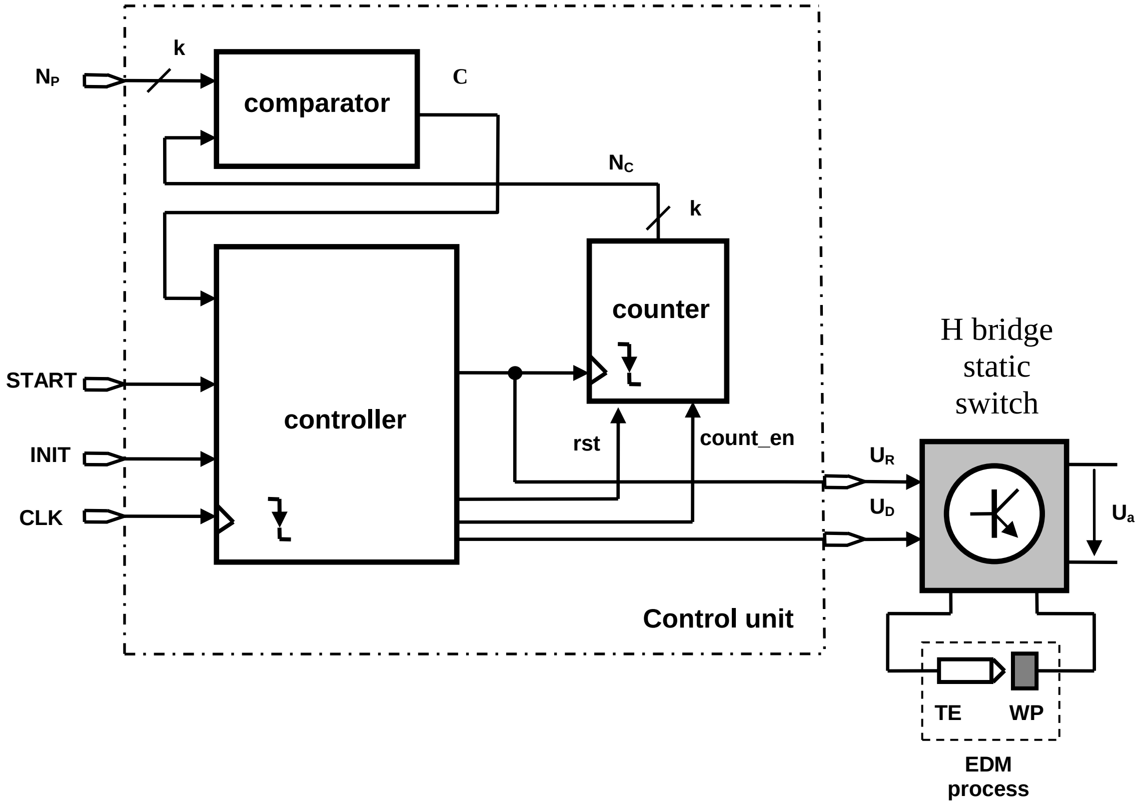

Fig. 7 ***Bloc diagram of the pulse generator***

6. CONCLUSION

The described pulse generator offers the possibility to study and test the effect of alternative pulses during the pre-ignition phase on the EDM elementary process. It is a possibility to increase the rate of electricl discharges in the dielectric liquid. Using programmable circuits and VHDL design techniques it becomes relatively easy to realize a pulse generator which can deliver a train with a programmable number of pulses.

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